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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/669,247
Filing Date: September 24, 2003
Appellant(s): LEA ET AL.

**Peter Kraguljac**
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed **10/14/2008** appealing from the Office action mailed **6/30/2008**.

**(1) Real Party in Interest**

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249, Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 6,697,898 | SHISHIZUKA | 2-2004 |
| 2003/0231330 | WESTERVELT | 12-2003 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

I. The objection to claim 15 has been withdrawn. The Examiner agrees with the Appellant that the antecedent to "the image data page" is in claim 15 and is correct.

II. Claims 1 – 4, 6 - 8, 10 - 12, 16 – 20, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over **SHISHIZUKA [US Patent 6,697,898 B1]** in view of **WESTERVELT [US Patent Application 2003/0231330 A1].**

As for claim 1, SHISHIZUKA teaches an image forming device comprising:

**a scanner configured to scan one or more objects and generate image data representing each of the one or more objects**

**[Fig. 2,** scanner **203**; **Fig. 4** also shows an interface to the scanner labeled "VIDEO I/F TO SCANNER" from the "DoEngine"**];**

**a memory configured to store each of the image data as a page of data**

**[Fig. 108,** RAM **203a** which contains "PAGE MEMORY" **511** shown in **Fig. 111;** also referred to as "SDRAM"; **col. 66, line 50];**

**a *page frame memory* configured to store *a page of* data, copied from the memory, that is to be imaged**

**[**SHISHIZUKA teaches a "page frame memory" which operates with the "G bus and B bus configuration". As shown in **Fig. 77**, SHISHIZUKA teaches buffering the "page memory" data in a "printer FIFO" which is contained in a printer image data transfer FIFO controller 6603. "This controller consists of a FIFO which is a buffer to transfer image data to the printer by way of the GBI (G bus/B bus I/F) and a circuit which controls the FIFO"; **col. 44, lines 14 – 18.** As shown in **Fig. 66,** the FIFO controller 6603 is a component of the "printer controller" **4303**; **col. 4, line 61.** As shown in **Fig. 4** and **Fig. 91,** the "printer controller" **4303** is a component of the "DoEngine"**];**

**an imaging mechanism configured to receive the *page of* data from the *page frame memory* and generate an image from the *page of* data onto a print media**

**[Fig. 111,** Printer **512; Fig. 4** also shows an interface to the printer labeled "VIDEO I/F TO PRINTER" from the "DoEngine"**];**

**and a dual bus system configured to allow parallel transmission of data where the image data can be transmitted from the scanner to the memory simultaneously with transmitting the *page of* data from the *page frame memory* to the imaging mechanism**

**[**The DoEngine is a "single-chip scanning and printing engine"; **col. 6, lines 57 – 58.** It has "two independent buses in its chip, namely an IO bus (B bus) which connects universal IO core and a graphics bus (G bus) which is optimized to transfer … image data"; **col. 7, lines 21 – 24.**

With reference to **Fig. 91,** SHISHIZUKA illustrates a "copy mode in which an image is copied by transferring image data from the scanner controller to the printer controller by way of a memory"; **col. 5, lines 51 – 54.**

SHISHIZUKA teaches, "The scanner controller (SCC) acquires the image data in synchronization with the timing signals" VSYNC and HSYNC; **col. 66, lines 44 – 46.** The GBI_SCC (i.e., the scanner G bus/B bus interface) "performs the DMA

transfer of acquired image data to the memory controller (MC) 403. The image data transferred by DMA is written by the MC 403 *into the SDRAM*"; **col. 66, lines 46 – 50.**

"When an amount of the image data written into the SDRAM reaches to a level sufficient to buffer a difference between the data transfer speeds of the scanner and the printer, image data transfer to the printer is started"; **col. 66, lines 50 – 53.**

"The printer controller (PRC) transfers the image data to the printer. By the DMA transfer of the GBI_PRC" (i.e., the printer G bus/B bus interface), "the *printer controller (PRC)* inputs the image data written in the SDRAM sequentially into the *internal FIFO*. Simultaneously, the printer controller (PRC) outputs the vertical synchronous signal (VSYNC) to the printer. Thereafter, the horizontal synchronous signal (HSYNC) and the video clock are input from the printer. In synchronization with the HSYNC and the video clock, the printer controller *outputs the image data from the internal FIFO to the printer*"; **col. 66, lines 58 – 67.**

Therefore, SHISHIZUKA teaches a first bus *between the scanner and the (SDRAM) memory* (i.e., from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" **4302** to *either* of the G bus or B bus (by means of a "G

Bus/B Bus I/F" **4301A**) to a "System Bus Bridge" **402,** "MC Bus", "SDRAM & ROM Controller (MC)" **403,** and "Memory BUS", all shown in **Fig. 4**) and a second bus *between the page frame memory and the imaging mechanism* (i.e., from the "Printer Controller" **4303** containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in **Fig. 4**).

Data can be transmitted from the scanner to (SDRAM) memory via the first bus while simultaneously transmitting data from the page frame memory to the printer via the second bus.**]**

However, SHISHIZUKA does not specifically teach

**a *page frame memory* configured to store a *page of* data**

WESTERVELT teaches a "page frame memory" which can be configured to store "a scanline, band, page or plane" of data; **page 6, paragraph 124, lines1 – 4.** "The actual pixel map images to be printed are transferred from the buffers 341 to DMA hardware or a FIFO buffer 353 for transfer to a printer by operation of output interface 347, output interrupt handler 349, graphic processors 337 and resource manager 343"; **col. 6, paragraph 121, lines 9 – 13.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of WESTERVELT with those of SHISHIZUKA and

configure *the size of* a "page frame memory" to store an amount of data (i.e., a scanline, band, *page* or plane) so as to maintain a balance between a level of system performance for the intended imaging mechanism and system cost. That is, the size of the page frame memory is a design choice.

Regarding claim 2, SHISHIZUKA further teaches the device of claim 1 where

**the dual bus system includes a first bus connected to communicate data between the scanner and the memory**

**[**As noted for claim 1, this bus extends from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" **4302** to either of the G bus or B bus (by means of a "G Bus/B Bus I/F" **4301A**) *and is* connected to SDRAM by means of a "System Bus Bridge" **402**, "MC Bus", "SDRAM & ROM Controller (MC)" **403**, and "Memory BUS", all shown in **Fig. 4]**,

**and a second bus, independent from the first bus, connected to communicate data between the page frame memory and the imaging mechanism**

**[**As noted for claim 1, this bus extends from the "Printer Controller" **4303** containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in **Fig. 4].**

Regarding claim 3, SHISHIZUKA further teaches the device of claim 2 where

**the first bus is configured to allow image data to be loaded into the memory independent of transmitting data from the *page frame* memory to the imaging mechanism**

**[**As noted for claim 1, once the page frame memory contains data for the imaging mechanism, data can be sent from the page frame memory (i.e., the printer controller's FIFO) independently of and simultaneously with loading image data from the scanner to the (SDRAM) "memory" since the first bus and second bus are separate busses**].**

Regarding claim 4, SHISHIZUKA further teaches the device of claim 2 further comprising:

**a first processor configured to control communication of the image data to the memory**

**[Fig. 4,** scanner controller **4302]**;

**and a second processor configured to control communication of the *page of* data from the *page frame* memory to the imaging mechanism**

**[Fig. 4,** printer controller **4303].**

Regarding claim 6, SHISHIZUKA further teaches the device of claim 4 where

**the first and second processors include application specific integrated circuits**

**[**Both first (i.e., scanner controller) and second (i.e., printer controller) processors are contained in the "DoEngine" application-specific IC (ASIC). "The DoEngine is a large-scale ASIC"; **col. 63, line 35].**

Regarding claim 7, SHISHIZUKA *does not specifically teach* the device of claim 1 where

**the *page frame memory* is configured to store *one or more pages of* *data* as one or more units**

However, as noted for claim 1, WESTERVELT teaches that a printer controller FIFO may store a "scanline, band, *page* or plane" of data at a time.

Regarding claim 8, SHISHIZUKA further teaches the device of claim 1 where

**the dual bus system is configured to communicate data by direct memory access**

**[**"The GBI_SCC performs the DMA transfer of acquired image data to the memory controller (MC) 403. The image data transferred by DMA is written by the MC 403 into the SDRAM"; **col. 66, lines 46 – 50.**

"By the DMA transfer of the GBI_PRC, the printer controller (PRC) inputs the image data written in the SDRAM sequentially into the internal FIFO"; **col. 66, lines 59 - 61].**

Regarding claim 10, SHISHIZUKA further teaches the device of claim 1 where

**the *page of* data includes at least three planes of color data**

**[Fig. 44,** video RGB (red, green, blue) image data from the "scanner device I/F" **4401].**

Regarding claim 11, SHISHIZUKA teaches a method of processing image data in an image forming device, the method comprising:

**scanning one or more sheets of print media and generating one or more image data pages;**

**loading the one or more image data pages into a memory;**

**[**SHISHIZUKA teaches, "The scanner controller (SCC) acquires the image data in synchronization with the timing signals" VSYNC and HSYNC; **col. 66, lines 44 – 46.** The GBI_SCC (i.e., the scanner G bus/B bus interface) "performs the DMA transfer of acquired image data to the memory controller (MC) 403. The image data transferred by DMA is written by the MC 403 *into the SDRAM*"; **col. 66, lines 46 – 50.]**

**copying a first image data *page* into a *page frame* memory from the memory to prepare for imaging**

**[**"When an amount of the image data written into the SDRAM reaches to a level sufficient to buffer a difference between the data transfer speeds of the scanner and the printer, image data transfer to the printer is started"; **col. 66, lines 50 – 53.**

"The printer controller (PRC) transfers the image data to the printer. By the DMA transfer of the GBI_PRC" (i.e., the printer G bus/B bus interface), "the *printer controller (PRC)* inputs the image data written in the SDRAM sequentially into the *internal FIFO*"; **col. 66, lines 58 – 61];**

**and transmitting the first image data page for imaging to an imaging mechanism where the transmitting occurs in parallel with the loading**

**[**"Simultaneously, the printer controller (PRC) outputs the vertical synchronous signal (VSYNC) to the printer. Thereafter, the horizontal synchronous signal (HSYNC) and the video clock are input from the printer. In synchronization with the HSYNC and the video clock, the printer controller *outputs the image data from the internal FIFO to the printer*"; **col. 66, lines 62 – 67.**

Therefore, SHISHIZUKA teaches a first bus *between the scanner and the (SDRAM) memory* (i.e., from the interface "VIDEO I/F TO SCANNER" to the

"Scanner Controller" **4302** to *either* of the G bus or B bus (by means of a "G Bus/B Bus I/F" **4301A**) to a "System Bus Bridge" **402,** "MC Bus", "SDRAM & ROM Controller (MC)" **403,** and "Memory BUS", all shown in **Fig. 4**) and a second bus *between the page frame memory and the imaging mechanism* (i.e., from the "Printer Controller" **4303** containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in **Fig. 4**).

Data can be transmitted from the scanner to (SDRAM) memory via the first bus while simultaneously transmitting data from the page frame memory to the printer via the second bus.**]**

However, SHISHIZUKA *does not specifically teach*

**copying a first image data *page* into a *page frame* memory from the memory to prepare for imaging**

WESTERVELT teaches a "page frame memory" which can be configured to store "a scanline, band, page or plane" of data; **page 6, paragraph 124, lines1 – 4.** "The actual pixel map images to be printed are transferred from the buffers 341 to DMA hardware or a FIFO buffer 353 for transfer to a printer by operation of output interface 347, output interrupt handler 349, graphic processors 337 and resource manager 343"; **col. 6, paragraph 121, lines 9 – 13.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of WESTERVELT with those of SHISHIZUKA and configure *the size of* a "page frame memory" to store an amount of data (i.e., a scanline, band, *page* or plane) so as to maintain a balance between a level of system performance for the intended imaging mechanism and system cost. That is, the size of the page frame memory is a design choice.

Regarding claim 12, SHISHIZUKA further teaches the method of claim 11 further including

> **converting the first image data page into print ready data before transmitting for imaging**
>
> **[**As shown in **Fig. 68**, Printer Video Clock Unit **6602** converts 64-bit image data to 24-bit RGB image data; a "Printer Video Data Width Converter" **6083** "is a block which converts image data sent in a 64-bit width from the I/F bus into RGB 24 bits, white-black 8 bits and white-black 1 bit dependently on a mode"; **col. 42, lines 42 - 46].**

Regarding claim 16, SHISHIZUKA further teaches the method of claim 11 further including

> **sequentially copying the *one or more image data pages* from the memory to the *page frame* memory to prepare for imaging**

**[**SHISHIZUKA teaches a "page frame memory" which operates with the "G bus and B bus configuration". As shown in **Fig. 77**, SHISHIZUKA teaches buffering the "page memory" data in a "printer FIFO" which is contained in a printer image data transfer FIFO controller **6603**. "This controller consists of a FIFO which is a buffer to transfer image data to the printer by way of the GBI (G bus/B bus I/F) and a circuit which controls the FIFO"; **col. 44, lines 14 – 18**. As shown in **Fig. 66**, the FIFO controller **6603** is a component of the "printer controller" **4303**; **col. 4, line 61**. As shown in **Fig. 4** and **Fig. 91**, the "printer controller" **4303** is a component of the "DoEngine"**].**

However, SHISHIZUKA *does not specifically teach*

**sequentially copying the *one or more image data pages***

As noted for claim 11, WESTERVELT teaches a "page frame memory" which can be configured to store "a scanline, band, page or plane" of data; **page 6, paragraph 124, lines1 – 4.** "The actual pixel map images to be printed are transferred from the buffers 341 to DMA hardware or a FIFO buffer 353 for transfer to a printer by operation of output interface 347, output interrupt handler 349, graphic processors 337 and resource manager 343"; **col. 6, paragraph 121, lines 9 – 13.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of WESTERVELT with those of SHISHIZUKA and

configure *the size of* a "page frame memory" to store an amount of data (i.e., a scanline, band, *page* or plane) so as to maintain a balance between a level of system performance for the intended imaging mechanism and system cost. That is, the size of the page frame memory is a design choice.

Regarding claim 17, SHISHIZUKA teaches a system for formatting image data for an image forming device, the system comprising:

**a first data bus**

**[**As noted for claim 1, this bus extends from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" **4302** to either of the G bus or B bus (by means of a "G Bus/B Bus I/F" **4301A**) *and is* connected to SDRAM by means of a "System Bus Bridge" **402,** "MC Bus", "SDRAM & ROM Controller (MC)" **403,** and "Memory BUS", all shown in **Fig. 4];**

**a first memory configured to store image data pages, the first memory being configured to receive the image data pages over the first data bus [Fig. 108,** RAM **203a** which contains "PAGE MEMORY" **511** shown in **Fig. 111;** also referred to as "SDRAM"; **col. 66, line 50];**

**a second memory configured to load *a page of* data that is to be imaged, the *page of* data being received from the first memory**

**[**SHISHIZUKA teaches a "page frame memory" which operates with the "G bus and B bus configuration". As shown in **Fig. 77**, SHISHIZUKA teaches buffering the "page memory" data in a "printer FIFO" which is contained in a printer image data transfer FIFO controller 6603. "This controller consists of a FIFO which is a buffer to transfer image data to the printer by way of the GBI (G bus/B bus I/F) and a circuit which controls the FIFO"; **col. 44, lines 14 – 18.** As shown in **Fig. 66,** the FIFO controller 6603 is a component of the "printer controller" **4303**; **col. 4, line 61.** As shown in **Fig. 4** and **Fig. 91,** the "printer controller" **4303** is a component of the "DoEngine"**];**

**and a second data bus configured to communicate the *page of* data from the second memory to an imaging mechanism**
**where the *page of* data can be transmitted to the imaging mechanism in parallel with the first memory receiving the image data pages.**
**[**As noted for claim 1, this bus extends from the "Printer Controller" **4303** containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in **Fig. 4.**

Since the first and second data busses are separate, data can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame memory to the printer.**]**

However, SHISHIZUKA *does not specifically teach*

**a second memory configured to load *a page of* data that is to be imaged, the *page of* data being received from the first memory**

WESTERVELT teaches a "page frame memory" which can be configured to store "a scanline, band, page or plane" of data; **page 6, paragraph 124, lines1 – 4.** "The actual pixel map images to be printed are transferred from the buffers 341 to DMA hardware or a FIFO buffer 353 for transfer to a printer by operation of output interface 347, output interrupt handler 349, graphic processors 337 and resource manager 343"; **col. 6, paragraph 121, lines 9 – 13.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of WESTERVELT with those of SHISHIZUKA and configure *the size of* a "page frame memory" to store an amount of data (i.e., a scanline, band, *page* or plane) so as to maintain a balance between a level of system performance for the intended imaging mechanism and system cost. That is, the size of the page frame memory is a design choice.

Regarding claim 18, SHISHIZUKA further teaches the system as set forth in claim 17 further including

**an imaging processor configured to process the page of data from the second memory into print ready data that can be processed by the imaging mechanism**

**[**As shown in **Fig. 68**, Printer Video Clock Unit **6602** converts 64-bit image data to 24-bit RGB image data; a "Printer Video Data Width Converter" **6083** "is a block which converts image data sent in a 64-bit width from the I/F bus into RGB 24 bits, white-black 8 bits and white-black 1 bit dependently on a mode"; **col. 42, lines 42 - 46].**

Regarding claim 19, SHISHIZUKA further teaches the system as set forth in claim 18 where

**the imaging processor includes one or more logic circuits each configured to process one plane of color data from the page of data**

**[**As shown in **Fig. 68**, Printer Video Clock Unit **6602** converts 64-bit image data to 24-bit RGB image data; a "Printer Video Data Width Converter" **6083** "is a block which converts image data sent in a 64-bit width from the I/F bus into RGB 24 bits, white-black 8 bits and white-black 1 bit dependently on a mode"; **col. 42, lines 42 – 46.**

**Fig. 71A** and **Fig. 71B** illustrate separate functional blocks which produce the above-mentioned "RGB" (red, green, blue) and "B/W" (black and white) printer data**].**

Regarding claim 20, SHISHIZUKA further teaches the system as set forth in claim 17 where

**the first data bus is in data communication with a scanning device configured to scan objects and generate an image data page including color data representing each scanned object**

**[Fig. 2,** scanner **203**; also, shown in **Fig. 4** is a "VIDEO I/F TO SCANNER"; the first bus extends from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" **4302** to either of the G bus or B bus (by means of a "G Bus/B Bus I/F" **4301A**) *and is* connected to SDRAM by means of a "System Bus Bridge" **402,** "MC Bus", "SDRAM & ROM Controller (MC)" **403,** and "Memory BUS", all shown in **Fig. 4.**

**Fig. 44** show a block diagram of the scanner controller (**Fig. 4** Scanner Controller **4302**) and illustrates color RGB 8-bit data being acquired from the "Scanner Device I/F" **4401].**

Regarding claim 22, SHISHIZUKA further teaches the system as set forth in claim 17 where

**the system is configured to copy an image data page from the first memory to the second memory by direct memory access**

**[**"The GBI_SCC performs the DMA transfer of acquired image data to the memory controller (MC) 403. The image data transferred by DMA is written by the MC 403 into the SDRAM"; **col. 66, lines 46 – 50**. "By the DMA transfer of the GBI_PRC, the printer controller (PRC) inputs the image data written in the SDRAM sequentially into the internal FIFO"; **col. 66, lines 59 - 61].**

Regarding claim 23, SHISHIZUKA further teaches the system as set forth in claim 17 where

**the system is configured to process image data pages as one or more data units**

**[Fig. 111** shows the "detailed software structure of the peripheral device in the information processing system" and how the software creates "jobs". With reference to **Fig. 111**, SHISHIZUKA further teaches a "composite copying job" which is "divided into a scanning job and printing job"; **col. 72, lines 38 – 39**. Further, "a device is assigned to the divided job in units of pages to process the job" (**col. 72, lines 40 – 42**)**].**

III. Claims 5, 9, 13, 14, 15 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **SHISHIZUKA [US Patent 6,697,898 B1]** in view of **WESTERVELT [US Patent Application 2003/0231330 A1]** and well-known prior art**.**

Regarding claim 5, SHISHIZUKA *does not specifically teach* the device of claim 4 where

**the second processor is *configured to decompress the page of data and transmit pulse modulated wave patterns* to the imaging mechanism based on the decompressed page of data**

However, SHISHIZUKA does teach that the "DoEngine can be combined with a rendering engine having a PCI bus interface and a compression/elongation engine"; **col. 7, lines 18 – 20**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add a compression/de-compression engine in order to efficiently use available RAM and external storage (e.g. a hard disk).

Regarding claims 9, SHISHIZUKA *does not specifically teach* the device of claim 1 further including

**a storage device *configured to store image data from the scanner once the memory is full*.**

In **Fig. 108**, SHISHIZUKA shows an "external storage device" **204a** "such as a hard disk" (**col. 70, lines 64 – 67**) and teaches that it may be used to store scanned image data; **col. 72, lines 9 – 10.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the storage disk device to "store overflow image data pages after the first memory is at capacity".

Regarding claim 13, SHISHIZUKA *does not specifically teach* the method of claim 11 further including

> ***holding the first image data page in the page frame memory until the imaging mechanism is ready to print*.**

However, SHISHIZUKA does teach that the print controller control register 6604 includes a "printer device status register"; **col. 44, line 45.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to check the printer device status register and confirm that the printer was in a state to receive data. For example, if the printer were in an error state (e.g. a paper jam), image data would be held in the page frame memory until the error condition cleared.

Regarding claim 14, SHISHIZUKA *does not specifically teach* the method of claim 11 further including

> ***loading one or more image data pages into a mass storage device once the memory is full*.**

In **Fig. 108**, SHISHIZUKA shows an "external storage device" **204a** "such as a hard disk" (**col. 70, lines 64 – 67**) and teaches that it may be used to store scanned image data; **col. 72, lines 9 – 10.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the storage disk device to "store overflow image data pages after the first memory is at capacity".

Regarding claim 15, SHISHIZUKA *does not specifically teach* the method of claim 11 further including

> ***removing an image data page from the memory after the image data page has been imaged and outputted from the image forming device*.**

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to either remove or overwrite the image data from memory in order to re-use the memory for subsequent pages.

Regarding claim 21, SHISHIZUKA *does not specifically teach* the system as set forth in claim 17 further including

> **a storage disk device *configured to store overflow image data pages after the first memory is at capacity***

In **Fig. 108**, SHISHIZUKA shows an "external storage device" **204a** "such as a hard disk" (**col. 70, lines 64 – 67**) and teaches that it may be used to store scanned image data; **col. 72, lines 9 – 10.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the storage disk device to "store overflow image data pages after the first memory is at capacity".

**(10) Response to Argument**

Regarding claim 1, with respect to Appellant's argument that

> *the "arrangement of elements, connections there between, and configuration of the dual bus is not taught or suggested by the references";* **page 12 of the Appeal Brief, 2nd paragraph,**
>
> *and "[a] page frame memory (being a separate element from the cache memory 403) is not present and not part of the G bus and B bus configuration. Thus, the claimed page frame memory and the claimed arrangement with the recited dual bus system is not taught by the G and B buses of SHISHIZUKA"*; **page 12 of the Appeal Brief, 3rd paragraph.**

has been considered.

In reply,

SHISHIZUKA cites, "This controller consists of a FIFO which is a buffer to transfer image data to the printer by way of the GBI (G bus/B bus I/F) and a circuit which controls the FIFO"; **col. 44, lines 14 – 18.** As shown in **Fig. 66,** the FIFO controller 6603 is a component of the "printer controller" **4303**; **col. 4, line 61.** As shown in **Fig. 4** and **Fig. 91,** the "printer controller" **4303** is a component of the "DoEngine".

*That is, the printer FIFO is an element that is separate from the "cache memory 403".*

In addition, SHISHIZUKA's "printer FIFO" (i.e., "page frame memory") is contained in a printer image data transfer FIFO controller 6603 which, in turn, is *connected to the G and B buses by means of the GBI (G bus/B bus I/F) interface*.

SHISHIZUKA teaches a first bus *between the scanner and the (SDRAM) memory* that utilizes *either* of the G bus or B bus and a second bus *between the page frame memory and the imaging mechanism* (i.e., from the "Printer Controller" **4303** containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in **Fig. 4**).

*That is, the second bus between the page frame memory and the imaging mechanism does not utilize either of the G bus or B bus.*

Regarding claim 1, with respect to Appellant's argument that

*"different components from SHISHIZUKI" have been cited "as being a first and second bus that teach the claimed dual bus system"*; **page 12 of the Appeal Brief, 4th paragraph,**

*and regarding the "scanner video I/F connections and components" shown in* ***Fig. 45*** *of SHISHIZUKA and the "printer controller 4303 components and connections including the printer device I/F" shown in* ***Figs. 66 – 67****of SHISHIZUKA, the multiple channels involved and multiple communication channels there between (e.g. different signal paths) are shown to pass different signals between each other over the different communication channels. This is a hodgepodge of components that fails to teach or suggest to one of ordinary skill in the art the actual claimed configuration";* **page 13, 3rd paragraph.**

has been considered.

In reply,

SHISHIZUKA teaches a first bus *between the scanner and the (SDRAM) memory* (i.e., from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" **4302** to *either* of the G bus or B bus (by means of a "G Bus/B Bus I/F" **4301A**) to a "System Bus Bridge" **402,** "MC Bus", "SDRAM & ROM Controller (MC)" **403,** and "Memory BUS", all shown in **Fig. 4**) and a second bus *between the page frame memory and the imaging mechanism* (i.e., from the "Printer Controller" **4303** containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in **Fig. 4**).

Data can be transmitted from the scanner to (SDRAM) memory via the first bus while simultaneously transmitting data from the page frame memory to the printer via the second bus.

SHISHIZUKA teaches that the DoEngine's "dual-bus [i.e., G-bus/B-bus] configuration", not to be confused with the first bus and second bus, "can solve the problem on occupation of the bus, and allows accessing the CPU and memory in parallel. *Data can be output in parallel with input of data*"; **col. 73, lines 31 – 34.**

With this configuration and with reference to **Fig. 113B**, SHISHIZUKA teaches that by using the DoEngine, a case "where processing is done *in parallel in units of pages* using a scanner and printer as device examples"; **col. 73, lines 44 – 46**

and **col. 73, line 60 – col. 74, line 10.** SHISHIZUKA further cites, "This configuration is *different from the prior art* in that *input data and output data can be processed in parallel* and the trap of data is cancelled"; **col. 74, lines 13 – 15.**

It should be noted that SHISHIZUKA discloses "lower-level implementation details", whereas, Appellant discloses (in **Figs. 1** and **2**) "higher-level architectural diagrams". Therefore, care should be taken when comparing the two inventions.

For example, even though SHISHIZUKA's first and second buses comprise "multiple components", the Appellant also has indicated that "*it will be appreciated that any number and configuration of data busses may be used to accommodate desired functions or preference. The operation and directional flow of the image data will be further explained with reference to Figure 2*"; **page 8 of the original specification, paragraph 27, lines 6 – 8.**

This appears to be an admission that the actual implementation of the "higher-level architectural diagrams" requires additional components.

For example, Appellant's "second bus" **185** shown in **Fig. 1** is illustrated as being composed of *one section* between the "page frame memory" **170** and an "imaging processor" **180** (which converts the data page from the page frame

memory **170** to a "print ready engine format"; **page 7 of the original specification, paragraph 24, lines 1 - 3**), and *another section* between the "imaging processor" **180** and "imaging mechanism" **130.**

Access to a memory device is typically made by use of a "memory bus" consisting of an *address bus*, a *data bus* and control lines, whereas, *communications* with an "imaging mechanism" is typically made by a bus consisting of data and control lines. This suggests that the *two sections* of the "second bus" **185** may not be the same.

Similarly, Appellant's "first bus" **155** shown in **Fig. 1** is illustrated as being composed of *one section* between the "scanner" **110** and the "controller" **140**, and *another section* between the "controller" **140** and the "main memory" **150**. As noted, access to a memory device is typically made by use of a "memory bus" consisting of an *address bus*, a *data bus* and control lines, however, Appellant also suggests that "data pages can then be sent and loaded into a formatter 120 by, for example, *a FIREWIRE® bus or other type of bus using another desired communication protocol*"; **page 4, lines 25 – 27.** Similarly, this suggests that the *two sections* of the "first bus" **155** are not the same.

Regarding claim 1, with respect to Appellant's argument that

*the conclusion made that "'data can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame memory to the printer' is not supported by SHISHIZUKA and no citation to an actual teaching or suggestion in SHISHIZUKA is provided. Accordingly, SHISHIZUKA fails to teach or suggest the elements relied upon by the rejection and fails to teach or suggest the claim";* **page 13 of the Appeal Brief, 4th paragraph.**

has been considered.

In reply,

SHISHIZUKA teaches that the DoEngine's "dual-bus [i.e., G-bus/B-bus] configuration", not to be confused with the first bus and second bus, "can solve the problem on occupation of the bus, and allows accessing the CPU and memory in parallel. *Data can be output in parallel with input of data*"; **col. 73, lines 31 – 34.**

Specifically, with reference to **Fig. 113B**, SHISHIZUKA teaches that by using the DoEngine, a case "where processing is done *in parallel* in units of pages using a scanner and printer as device examples"; **col. 73, lines 44 – 46** and **col. 73, line 60 – col. 74, line 10.** SHISHIZUKA further cites, "This configuration is *different from the prior art* in that *input data and output data can be processed in parallel* and the trap of data is cancelled"; **col. 74, lines 13 – 15.**

Regarding claim 1, with respect to Appellant's argument that

> *since "claim 1 does not recite accessing a CPU and memory in parallel", therefore, "claim 1 is not taught or suggested";* **page 14 of the Appeal Brief, 1st paragraph**

has been considered.

In reply,

> This argument would appear to be not relevant in that SHISHIZUKA's invention may have additional capabilities *not cited in claim 1* but still teaches the claimed configuration of "*a first bus* ***between*** *a scanner and memory, and a second bus* ***between*** *a page frame memory and an imaging mechanism*".
>
> Even though SHISHIZUKA teaches "different components" as being a "first bus" and a "second bus", there should be no doubt that SHISHIZUKA teaches a "first bus between a scanner and memory, and a second bus between a page frame memory and an imaging mechanism".

Regarding claim 1, with respect to Appellant's argument concerning SHISHIZUKA's teaching in **col. 73, lines 33 – 34** (i.e., "*Data can be output in parallel with input of data*") that

> *"[t]his means that the scanner itself is scanning at the same time the printer is printing. However, the claim recites a configuration internal and in-between the scanner and printer, not the operation of the scanner and printer";* **page 14 of the Appeal Brief, 1st paragraph,**

and Appellant's argument concerning SHISHIZUKA's teaching in **col. 73, lines 41 – 42, 44 – 46** (i.e., the "*assignment and release of a device*") that

> *"this section describes the operation of the scanner scanning and the printer printing in parallel";* **page 14 of the Appeal Brief, 2nd paragraph**

have been considered.

In reply,

> Since SHISHIZUKA's invention is the "DoEngine" which is a "*single-chip scanning and printing engine*" (**col. 6, lines 57 – 58**) it would appear that the Appellant has mischaracterized SHISHIZUKA's invention because *it is the DoEngine that interfaces with and is "in-between the scanner and printer"* and which allows the scanner to scan at the same time the printer is printing.

Regarding claim 1, with respect to Appellant's argument that

> *"how the VSYNC and HSYNC signals are processed fail to teach or suggest simultaneous or parallel transmission of data by a dual bus transferring data from*

*page frame memory to the imaging mechanism while also transferring image data from a scanner to main memory";* **page 15 of the Appeal Brief, 1st paragraph**

has been considered.

In reply,

The claim rejections do not sole rely upon SHISHIZUKA's discussion of the vertical synchronous signals (VSYNC) and the horizontal synchronous signals (HSYNC).

The "mode 3" copying operation, as recited in the claim rejection, "is selected by the system which has a configuration wherein a vertical synchronous timing, a horizontal synchronous timing and a video data transfer speed are different from one another between the scanner and the printer"; **col. 66, lines 34 - 38.**

The recitation of the VSYNC and HSYNC signals was in relation to how "the scanner controller (SCC) acquires the *image data* in synchronization" with these timing signals, and how the printer controller "outputs the image data from the internal FIFO to the printer" in synchronization with these timing signals.

It should also be noted that the section from **col. 65, lines 10 – 30**, cited by Appellant on **page 15 of the Appeal Brief, 1st paragraph** pertains to a different "mode 1" copying operation, whereas, the section from **col. 66, lines 58 – 67**, cited by Appellant on **page 15 of the Appeal Brief, 1st paragraph** pertains to the aforementioned "mode 3" copying operation.

Regarding claim 1, with respect to Appellant's argument that

*since SHISHIZUKA cites in* ***col. 67, lines 1 – 12*** *that "the image data flow in a sequence …", therefore, "parallel transmission of data as claimed is not taught or suggested";* **page 15 of the Appeal Brief, 2nd paragraph**

has been considered.

In reply,

This appears to be a mischaracterization of SHISHIZUKA's invention. The sequence cited in **col. 67, lines 1 - 12** merely teaches how image data flows in from the scanner *through the DoEngine* and out to the printer. The "sequence" refers to the sequential order in which each of the elements of the DoEngine are utilized in transferring the image data from the scanner to the printer.

Regarding claim 1, with respect to Appellant's argument that

*"WESTERVELT fails to teach or suggest to one of ordinary skill how its FIFO buffer would be connected and where it would be connected into the DoEngine of SHISHIZUKA. Indeed the DoEngine already includes a cache memory 403 (figure 4) and the printer controller 4303 already includes a FIFO buffer 6608 (figure 66)";* **page 15, 4th paragraph.**

*"Thus, the motivation to combine provided by the Office Action (page 8, 3rd paragraph) is not supported by the references and contradicts the actual result of the proposed modification. Instead, the combination is made only by impermissible hindsight using the claims as a blueprint. The rejection is improper";* **page 16, 1st paragraph.**

has been considered.

In reply,

SHISHIZUKA teaches a "page frame memory" which operates with the "G bus and B bus configuration". As shown in **Fig. 77**, SHISHIZUKA teaches buffering the "page memory" data in a "printer FIFO" which is contained in a printer image data transfer FIFO controller 6603. "This controller consists of a FIFO which is a buffer to transfer image data to the printer by way of the GBI (G bus/B bus I/F) and a circuit which controls the FIFO"; **col. 44, lines 14 – 18.** As shown in **Fig. 66,** the FIFO controller 6603 is a component of the "printer controller" **4303**; **col.**

**4, line 61.** As shown in **Fig. 4** and **Fig. 91,** the "printer controller" **4303** is a component of the "DoEngine".

WESTERVELT teaches a "page frame memory" which can be configured to store "a scanline, band, *page* or plane" of data; **page 6, paragraph 124, lines1 – 4.**

SHISHIZUKA does not specifically teach a page frame memory (i.e., the "printer FIFO") as being configured to store *a page of data*.

However, WESTERVELT teaches that the size of the "printer FIFO" can be made to accommodate *not only pages of data* but also scanlines, bands or planes of data.

*That is, it would have been obvious to one of ordinary skill in the art at the time the invention was made to match the size of the "printer FIFO" with the "imaging mechanism".* For example, it is well-known that laser printers require page-sized memories, whereas, a scanning inkjet printer requires a smaller band-sized memory.

The question is not *how to connect* WESTERVELT's FIFO buffer into SHISHIZUKA's DoEngine but rather *how to adjust the size* of SHISHIZUKA's

"printer FIFO" relative to the "imaging mechanism". WESTERVELT provides this teaching.

Regarding claim 2, with respect to Appellant's argument that

*"no such first or second bus is taught or suggested";* **page 16, 3rd paragraph.**

has been considered with respect to **claim 1**.

Regarding claim 11, with respect to Appellant's argument that

*the Office Action's citation of SHISHIZUKA's timing signals VSYNC and HSYNC signals on* ***page 13*** *"are not image data pages that are generated from scanning sheets of print media as recited in the claim, and the timing signals are not image data pages loaded into a memory";* **page 17, 2nd paragraph.**

*"As such, the VSYNC and HSYNC timing signals, as well as the processing of the timing signals, are irrelevant to the claimed elements. Thus, the cited text fails to teach or suggest 'transmitting the first image data page for imaging to an imaging mechanism where the transmitting occurs in parallel with the loading' as recited in claim 11";* **page 17, 3rd paragraph.**

has been considered.

In reply,

The “mode 3” copying operation, as recited in the claim rejection, "is selected by the system which has a configuration wherein a vertical synchronous timing, a horizontal synchronous timing and a video data transfer speed are different from one another between the scanner and the printer"; **col. 66, lines 34 - 38.**

The recitation of the VSYNC and HSYNC signals was in relation to how “the scanner controller (SCC) acquires the *image data* in synchronization” with these timing signals, and how the printer controller “outputs the image data from the internal FIFO to the printer” in synchronization with these timing signals.

SHISHIZUKA teaches that “the image data is output in synchronization with these signals. The scanner controller (SCC) acquires the image data in synchronization with the timing signals” VSYNC and HSYNC; **col. 66, lines 43 – 46.**

SHISHIZUKA teaches that the DoEngine’s “dual-bus [i.e., G-bus/B-bus] configuration”, not to be confused with the first bus and second bus, “can solve the problem on occupation of the bus, and allows accessing the CPU and memory in parallel. *Data can be output in parallel with input of data*”; **col. 73, lines 31 – 34.**

Specifically, with reference to **Fig. 113B**, SHISHIZUKA teaches that by using the DoEngine, a case "where processing is done *in parallel* in units of pages using a scanner and printer as device examples"; **col. 73, lines 44 – 46** and **col. 73, line 60 – col. 74, line 10.** SHISHIZUKA further cites, "This configuration is *different from the prior art* in that input data and output data can be processed in parallel and the trap of data is cancelled"; **col. 74, lines 13 – 15.**

Regarding claim 17, with respect to Appellant's argument that

*"SHISHIZUKA fails to teach or suggest the recited arrangement of a first data bus, a second data bus, a first memory, a second memory, and parallel transmission of data between components as recited in claim 17";* **page 18, 2nd paragraph,**

*and with regards to WESTERVELT's teaching a FIFO buffer, "as explained under claim 1, the combined references still fail to establish a prima facie obviousness rejection";* **page 16, 3rd paragraph.**

has been considered with respect to **claims 1** and **2**.

Regarding claims 5, 9, 13, 14, 15 and 21 with respect to Appellant's argument that

*"the claimed elements are well-known. Authority must be produced to support the rejection. The rejection fails to point to concrete evidence in the record to support its findings";* **page 19 of the Appeal Brief, last paragraph**

has been considered.

In reply,

Claims 5, 9, 13 – 15 and 21 were rejected under 35 U.S.C. 103(a) as being unpatentable over SHISHIZUKA in view of WESTERVELT and well-known prior art in the second non-final office action. Appellant did not adequately traverse the official notice. MPEP 2144.03, section (C) states:

> To adequately traverse such a finding, an applicant must specifically point out the supposed errors in the examiner's action, which would include stating why the noticed fact is not considered to be common knowledge or well-known in the art.

That is, Appellant failed to state "why the noticed fact is *not considered to be common knowledge or well-known in the art*". Instead, Appellant only remarked that, "Shishizuka and Westervelt fail to establish a prima facie obviousness rejection of any claim. The deficiencies are not cured by what is alleged to be well known prior art. Thus prima facie obviousness rejection is not established by the references and the rejection is improper"; **page 16 of Applicant's remarks, dated April 24, 2008, last paragraph**.

In the Appeal Brief, **page 19, last paragraph**, Appellant further does not state "why the noticed fact is *not considered to be common knowledge or well-known in the art*".

Instead, Appellant remarks, "Appellant disputes that the claimed elements are well known. Authority must be produced to support the rejection. The rejection fails to point to concrete evidence in the record to support its findings".

Regarding claim 5, in addition to "decompressing the page of data", it would have been obvious to one of ordinary skill in the art at the time the invention was made to "*transmit pulse modulated wave patterns to the imaging mechanism based on the decompressed page of data*" because the concept of converting image data into pulse-width modulated signals to control a scanning laser is well-known in the art of electrostatic printing. It is also well-known in the art of thermal inkjet printing to convert image data into pulse-width modulated signals to control the heating elements in a print head. That is, it is well-known in the art to convert image data stored in a memory into electrical signals which can be used to place toner or ink onto a printing substrate (e.g., a sheet of paper).

Regarding claim 9, in addition, it would have been obvious to one of ordinary skill in the art at the time the invention was made to *store image data from the scanner in a storage device (e.g., a hard disk) once the memory (e.g., a semiconductor random-access memory, RAM) became full* so that a document whose image size would normally exceed the size of the memory could be scanned in its entirety by *overflowing image data pages into the storage device after the memory became full (or reached its capacity)*. In this way, the size of the *more expensive* semiconductor random-access

memory could be reduced compared to the *less expensive* hard disk storage device, thereby, achieving a lower overall systems cost.

Regarding claim 13, in addition, it is believed that *holding the first image data page in the page frame memory until the imaging mechanism is ready to print* is commonsense. If the imaging mechanism is not ready to print (e.g., it is "warming up"), the imaging mechanism can not "consume" or process the image data that is stored in the page frame memory. Therefore, it would make sense for the *first image data page to be held in the page frame memory until the imaging mechanism is ready to print*.

The Examiner is also familiar with the operation of a Canon imageRunner® 5000S digital copying machine at the U.S. Patent and Trademark Office that allows "reservation copies" to be made while the copying machine is "warming up". Specifically, when the copying machine is powered on, the first five pages of a document can be scanned and stored into a memory. In this state, the operation panel displays the messages, "Reservation copies can be made" and "printer is warming up". After the first five pages are scanned and stored into a memory, no further pages can be scanned until the digital copying machine is ready to print and consume the image data that is stored in the memory. After the stored image data is consumed and printed, additional pages of the document can then be scanned. That is, even this particular digital copying machine holds the first through fifth image data pages in a page frame memory until it is ready to print.

Regarding claim 14, similar to claim 9, it would have been obvious to one of ordinary skill in the art at the time the invention was made to *load one or more image data pages into a mass storage device (e.g., a hard disk) once the memory (e.g., a semiconductor random-access memory, RAM) became full* so that a document whose image size would normally exceed the size of the memory could be scanned in its entirety by *overflowing image data pages into the mass storage device after the memory became full (or reached its capacity)*. In this way, the size of the *more expensive* semiconductor random-access memory could be reduced compared to the *less expensive* hard disk storage device, thereby, achieving a lower overall systems cost.

Regarding claim 15, in addition, it is believed that *removing an image data page from the memory after the image data page has been imaged and outputted from the image forming device* is commonsense. Since the size of memory is not infinite, removing image data pages from the memory would be necessary in order to scan additional pages once the memory became full.

Regarding claim 21, similar to claims 9 and 14, it would have been obvious to one of ordinary skill in the art at the time the invention was made to *include a storage disk device (e.g., a hard disk) configured to store overflow image data pages after the first memory (e.g., a semiconductor random-access memory, RAM) is at capacity* so that a document whose image size would normally exceed the size of the memory could be

scanned in its entirety by *overflowing image data pages into the mass storage device after the memory became full (or reached its capacity)*. In this way, the size of the *more expensive* semiconductor random-access memory could be reduced compared to the *less expensive* hard disk storage device, thereby, achieving a lower overall systems cost.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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